

Dual Layer 3D-Stacked High Dynamic Range SPAD Pixel

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Abstract—A dual layer single photon avalanche diode (SPAD) pixel implemented in a 3D-stacked CMOS technology is presented. Two SPAD devices are arranged vertically such that the backside illuminated (BSI) top diode and the front side illuminated (FSI) bottom diode form a single pixel unit. The outputs of both $29 \mu\text{m}^2$ active area devices are connected to quench and processing electronic circuits on the bottom tier. Characterization results of both SPADs shows a peak photon detection probability (PDP) of 28% at 615 nm and 5% at 585 nm for the top and bottom devices respectively at 3 V excess bias. Dynamic range (DR) extension in single photon counting (SPC) mode by 15 dB and avoidance of pile-up conditions in time correlated single photon counting (TCSPC) mode are demonstrated. Angular response measurements of the pixel to incoming light are also presented. Both SPADs exhibit a low jitter of ~ 70 ps at 2 V excess bias and 773 nm showing no degradation to temporal resolution.

I. INTRODUCTION

Due to their high sensitivity, temporal resolution and integration in CMOS processes, SPAD devices have become the detectors of choice for a wide range of photon counting time-resolved scientific and consumer applications such as fluorescence lifetime imaging (FLIM) and light detection and ranging (LIDAR) respectively.

Intrinsically SPADs can offer a high dynamic range in excess of 100 dB bounded by the dark count rate (DCR) noise floor, the maximum attainable count rate determined by the detector's deadtime, and the recharge circuit configuration. Capturing the full DR is a pixel design challenge whereby a high bit depth digital counter is required resulting in a prohibitively large pixel pitch. Yet, such a pixel can be efficiently realized when implemented in advanced CMOS nodes including 40 nm [1].

When that is not applicable, typically in analogue pixel implementations due to the limited photon counting capacity, alternating the operation of the detector between integration and avalanche modes to extend the DR was proposed and demonstrated by [2]. By capturing standard images in photodiode (integration) mode and binary images in avalanche photodiode (APD) mode, an aggregate DR of 100dB was achieved. Alternatively, techniques for extending the DR via multiple exposures of oversampled binary SPAD image sensors without adjusting the device mode for operation were explored in [3].

Recent progress in integrating SPAD devices in industrial wafer scale 3D-stacked CMOS technologies gave way to compact, high photon counting capacity, and time-resolved capable imaging arrays [4]. While SPAD devices are conventionally

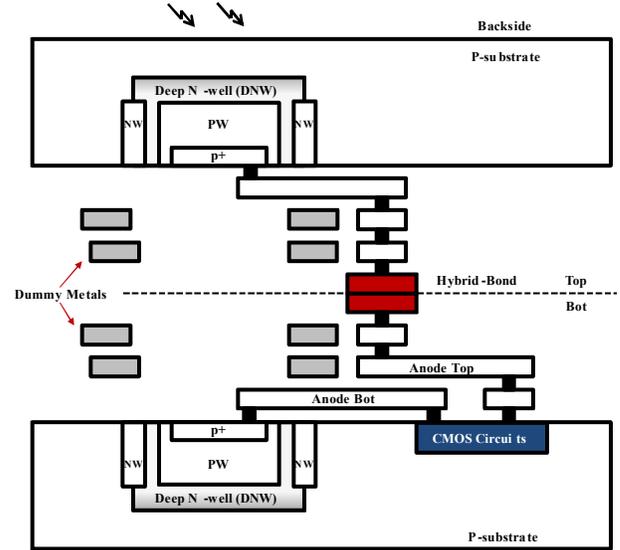


Fig. 1. Cross-section of the dual layer SPAD pixel.

implemented only in the top tier of a stacked sensor, the first dual layer SPAD array has been reported in [5]. However, this sensor was aimed at charged particle detection, and is not amenable to imaging applications due to the large backside thickness of the top tier ($280 \mu\text{m}$) and the metal shielding between the two layers.

Dual layer CMOS image sensors and concepts have been demonstrated for enhanced multi-band (RGB-IR) response [6], and low light color imaging [7]. The same techniques are applicable to SPAD image sensors, hence this paper presents the first dual layer imaging SPAD pixel for extended dynamic range in photon counting mode, and improved pile-up distortion in time-resolved scenarios.

II. PIXEL CONFIGURATION

A BSI top tier SPAD in a 90 nm imaging process and a FSI bottom tier SPAD in a 40 nm standard process, were designed such that they are vertically aligned forming a single pixel unit. Both SPADs have the same p-well (PW) to deep n-well (DNW) junction [4], [8] and an active area of $29 \mu\text{m}^2$. Metallization between the two SPADs on both tiers was avoided in order not to obscure the incoming light. In addition, the bottom tier dummy metal patterns were utilized to create a ring around the bottom SPAD to restrict its sensitivity to light passing through the top SPAD aperture. The top SPAD anode

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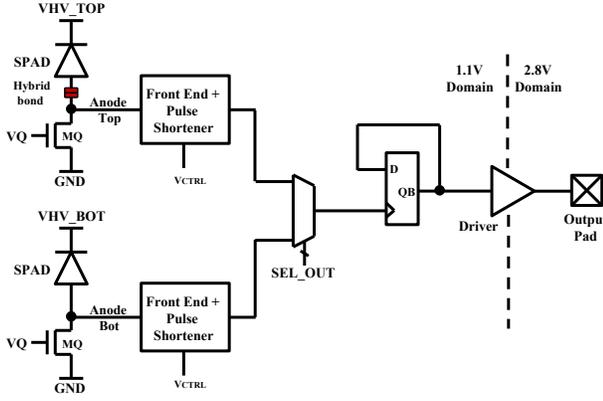


Fig. 2. Circuit diagram of the dual layer SPAD pixel.

was connected to bottom tier circuitry via a single hybrid-bond site. No active circuitry were integrated on the top tier. Fig. 1 shows the pixel cross-section.

Fig. 2 shows the bottom tier circuit diagram. Each SPAD front-end comprises a passive quench and recharge transistor followed by a pulse shortener. Each SPAD has a separate high voltage (VHV) supply, and VQ and VCTRL are fixed to 1.1 V and 0.55 V respectively in this test pixel due to the limited number of pad connections.

A multiplexer (MUX) selects between the output of each SPAD. This signal is then fed into a toggle flip-flop due to short SPAD pulses ($< 1 ns$ from extracted simulations) which cannot propagate through the output chain. An optimized output stage with $\sim 500 ps$ rise/fall time drives the passive output pad and its external load. A Xilinx based FPGA counter and a LeCroy WaveRunner 640z oscilloscope were used for characterization purposes.

III. PIXEL CHARACTERIZATION

The photon detection probability (PDP) of both SPADs was measured at 3 V excess bias voltage. Fig 3 shows the PDP versus wavelength. Similar to previous BSI 3D-stacked SPADs [4] the top tier device peak PDP is 28% at 615 nm with a clear cut-off in the blue region of the spectrum. On the other hand, the bottom tier device shows a peak PDP of only 5% at 585 nm due to the attenuation of the optical stack in top and bottom tiers.

Nevertheless this attenuation is beneficial in increasing the DR in single photon counting mode by switching the detector of choice between the two SPADs. Fig. 4 shows the count rate response of both SPADs versus optical power of a white LED source. It is evident that the bottom SPAD reaches saturation later on providing an additional 15 dB in DR over the intrinsic DR of the top SPAD. Both devices were operated at 2 V excess bias and reached a maximum count rate exceeding 100 Mcps indicating a deadtime of $\sim 3.5 ns$.

Table. I shows the dark count rate (DCR) measurements for four individual chips at excess voltage of 2 V and room temperature. The average DCR among the four top and bottom

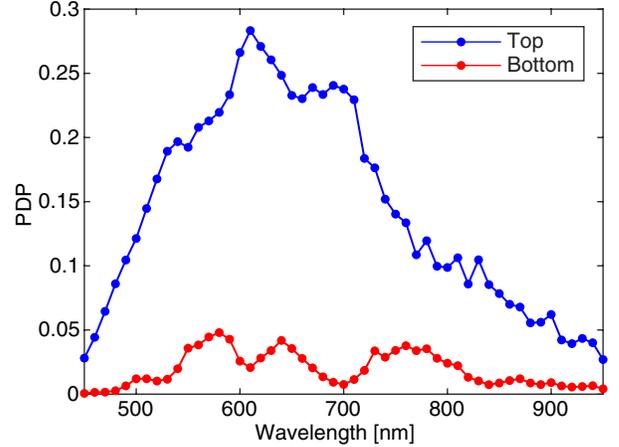


Fig. 3. Photon detection probability at excess bias of 3 V, wavelength step of 2 nm, and bandwidth of $\sim 2 nm$.

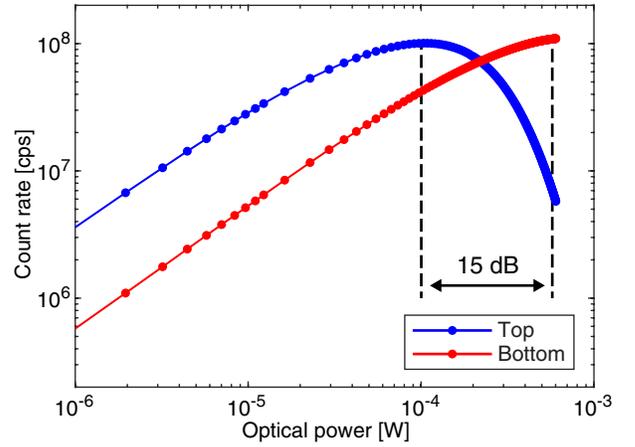


Fig. 4. Count rate versus optical power at 2 V excess bias.

SPADs is $0.04 cps/\mu m^2$, and $16.6 cps/\mu m^2$ respectively. Since the top SPAD is based on an optimized fabrication process, the the DCR and its variations among the 4 chips are smaller than the bottom SPAD. Note that the bottom SPAD is based on a standard CMOS process which is not optimized for low DCR. However, as the main application for this pixel structure is extending the DR, the DCR of the bottom SPAD is not of significant importance.

TABLE I
DARK COUNT RATE OF THE 3D SPAD IN CPS AT $V_{ex} = 2V$

Type	Chip			
	A	B	C	D
Top	1.36	1.06	1.24	1.28
Bottom	43.80	357.9	36.66	1485

Since high temporal resolution is one of the main desired features of SPADs, the jitter of both devices was measured at 2 V excess bias using a Hamamatsu PLP10 773 nm laser with a quoted jitter of 56 ps FWHM. Both devices exhibit a jitter of $\sim 70 ps$ FWHM in Fig. 5 without correcting for the laser

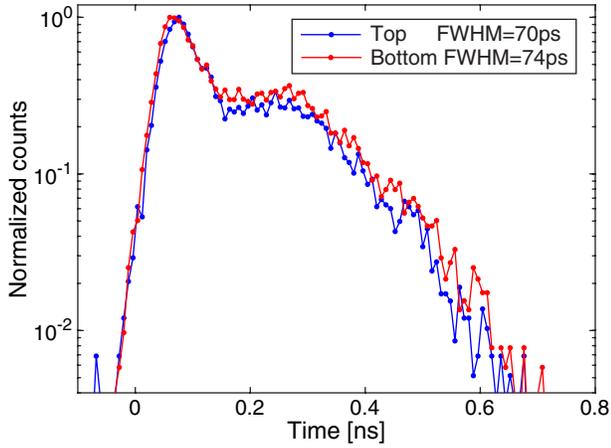


Fig. 5. The jitter histogram for the top and bottom SPADs at excess bias of $2V$, and wavelength of 773 nm .

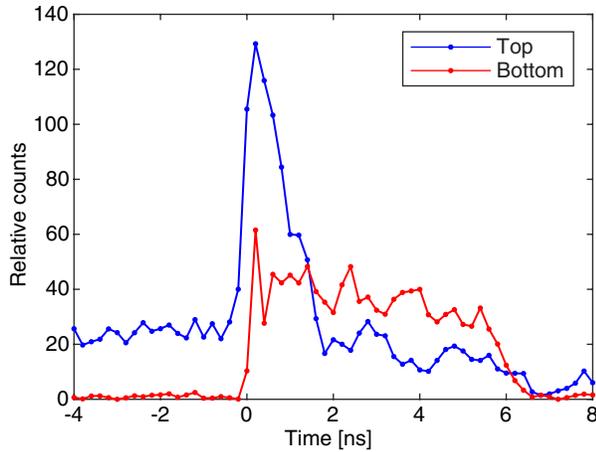


Fig. 6. The recovery of a 6 ns laser pulse under pile-up conditions.

or circuit contributions confirming the expected result that a dual layer pixel does not degrade the temporal performance.

In a time-resolved scenario, the effectiveness of recovering a laser pulse under pile-up conditions was investigated by operating the top SPAD under ambient conditions close to its saturation limit. A 6 ns PicoQuant 840 nm pulse was then introduced. Fig. 6 shows the distorted resolved pulse. By switching to the bottom tier SPAD, pile-up is avoided and the laser's pulse profile is clearly recovered.

Both SPADs are characterized for afterpulsing. Fig. 7 and Fig. 8 show the time interval histogram for the top and bottom SPADs respectively, when they are exposed to a low light level of approximately 100 kcps . The red solid line shows the statistical distribution of the time interval for an ideal SPAD which is exponential, however afterpulsing related pulses appear on shorter time intervals, resulting in a slightly distorted distribution. As the inset figures show a zoom in the horizontal axis of the histogram, It appears that the BSI follows the ideal distribution, whilst the FSI has more pulses than expected on the shorter time intervals. As a result, the

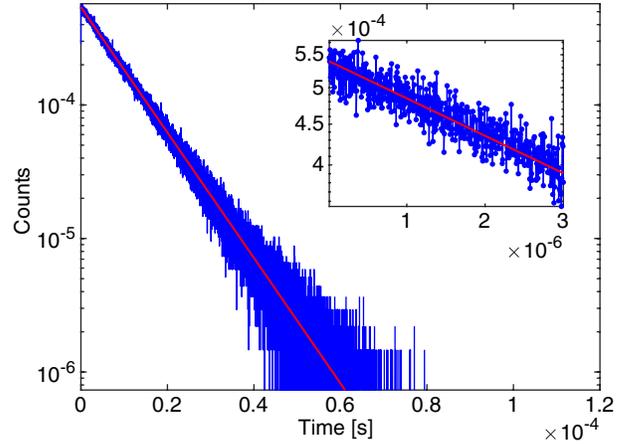


Fig. 7. Inter-pulse time distribution of the top SPAD when average count rate is 100 kcps . The red line shows the fitted distribution. The inset is a zoom on shorter time intervals.

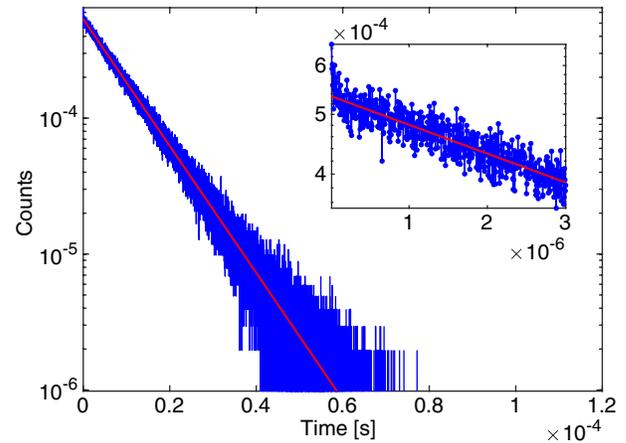


Fig. 8. Inter-pulse time distribution of the bottom SPAD when average count rate is 100 kcps . The red line shows the fitted distribution. The inset is a zoom on shorter time intervals.

ratio of pulses contributing to after-pulsing for the top SPAD are 0.1% and for the bottom SPAD are 0.4% .

Although the SPADs are electrically isolated from each other, optical cross-talk is possible due to secondary photon emission during the impact ionization process [9]. In order to measure this optical cross-talk, the count rate was measured only when either top or bottom SPADs were activated. The counts were measured again when both SPAD were activated. Fig. 9a and 9b show the count rate measurements for top and bottom SPADs respectively. Fig. 9c and 9d show an overlapped version of Fig. 9a and 9b respectively. It is clear from these measurements that the variations in the intensity of the light source is higher than the expected optical cross-talk. As a result, the optical cross-talk is smaller than 0.1% of total counts.

Moreover, the angular response of both SPADs to incident light was measured to evaluate the potential of using such a pixel in angle sensitive applications. For a fixed illumination

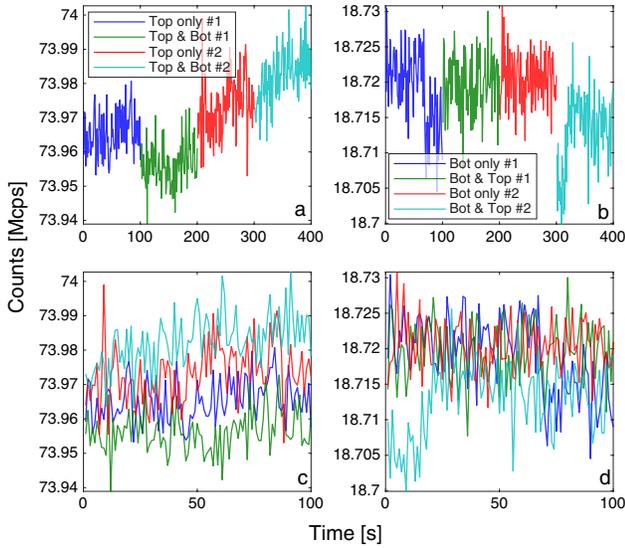


Fig. 9. The measurement of various activation configurations of the top and bottom SPADs.

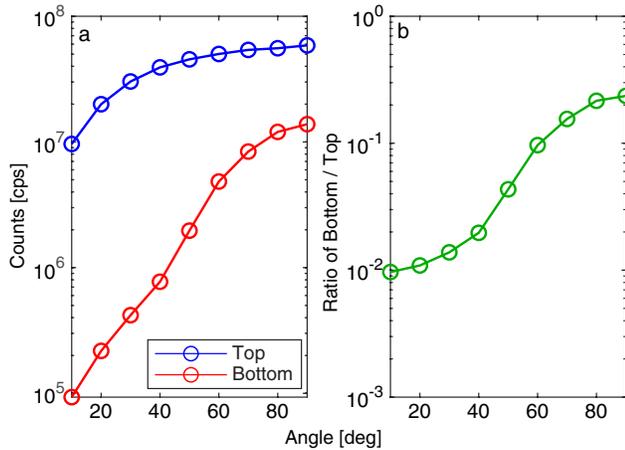


Fig. 10. The effect of incident light angle on (a) Count rate (b) Ratio of bottom to top SPAD count rates.

level where both SPADs are in the linear count rate region, the incident angle was varied across half an axis (since the test structure is symmetrical) and the count rates were recorded in Fig. 10. Relative to perpendicular incident light, the top SPAD exhibits a slow change in count rate due to the wide field of view while the bottom SPAD decreases at a faster rate due to the restricted field of view by the vertical metal structure surrounding the active area.

IV. DISCUSSION

The presented results provide proof of principle of a dual tier pixel and future developments in device structure such as reduced metal layers and engineered light pipes [10] would improve the performance of the bottom diode as well as implementing it in a SPAD specific 40 nm process [8]. A future version of this vertically integrated pixel with closer PDP

values at the wavelength of interest, better SPAD deadtime, and pulse shortener control can be applied in coincidence based TCSPC experiments and applications such as LiDAR [11]. Such a SPAD could also be advantageous in wavelength division multiplexing in optical communications in order to reduce the effect of deadtime on a SPAD array [12]. Trade-off between bottom tier SPAD and processing electronics areas is a challenge for 2-dimensional arrays which would necessitate a smaller bottom tier diode compared to the top one. However, a smaller bottom diode is advantageous to applications which only require an increased dynamic range. An alternative is three tier stacking [13] where the first two layers are dedicated for SPADs.

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